



SSC8162GS6

N-Channel Small Switching MOSFET with ESD Protection

Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D	ESD
60V	$\pm 12V$	1 Ω @10V	0.5A	500V
		1.5 Ω @4V5		

Description

This device is an N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

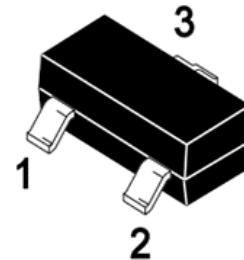
Applications

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers
- Display, Memories, Transistors, etc.
- Battery Operated System
- Solid-State Relays

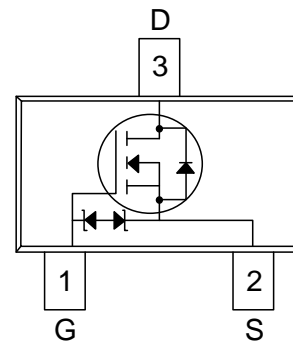
Ordering Information

Device	Package	Shipping
SSC8162GS6	SOT-23	3000/Reel

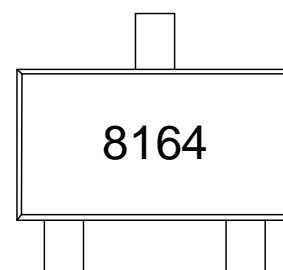
Pin configuration



SOT-23



Pin Configuration (Top View)



Marking



➤ **Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	60	V
V_{GSS}	Gate-to-Source Voltage	± 12	V
I_{D}	Continuous Drain Current ^a	0.5	A
I_{DM}	Pulsed Drain Current ^b	1	A
P_{D}	Power Dissipation ^c	0.85	W
P_{DSM}	Power Dissipation ^a	0.36	W
T_{J}	Operation junction temperature	$-55\sim 150$	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	$-55\sim 150$	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Maximum	Unit
$R_{\theta\text{JA}}$	Junction-to-Ambient Thermal Resistance ^a	360	$^{\circ}\text{C}/\text{W}$
$R_{\theta\text{JC}}$	Junction-to-Case Thermal Resistance	155	$^{\circ}\text{C}/\text{W}$

Note:

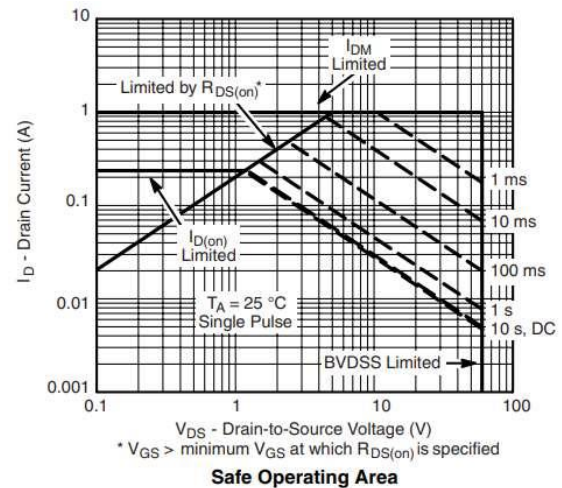
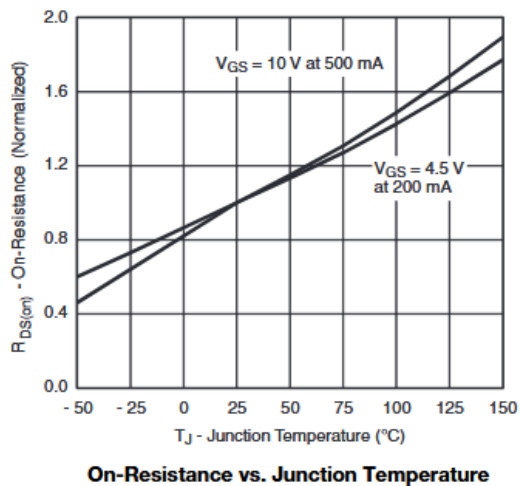
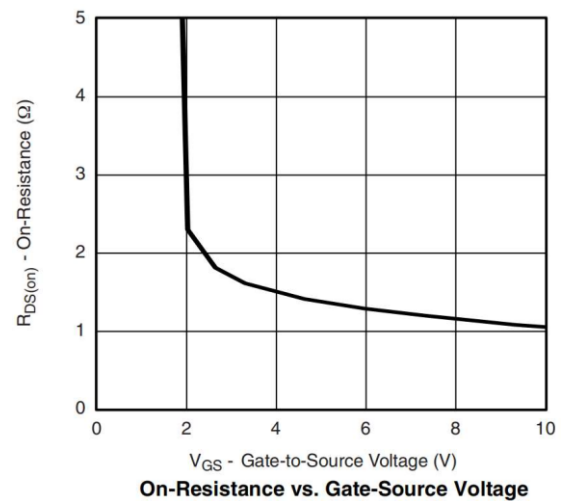
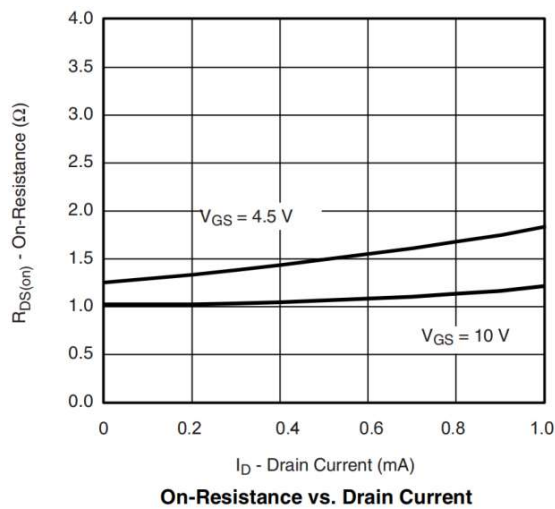
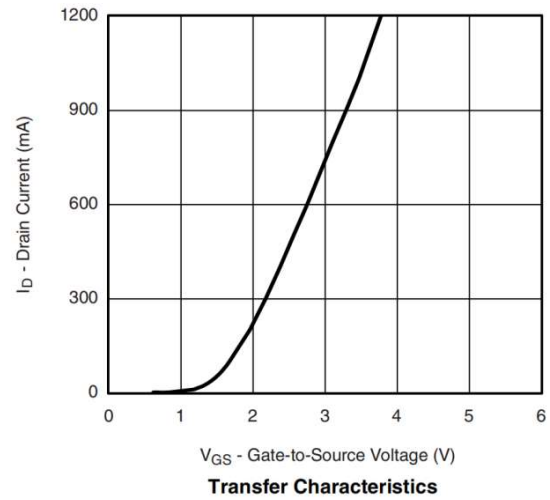
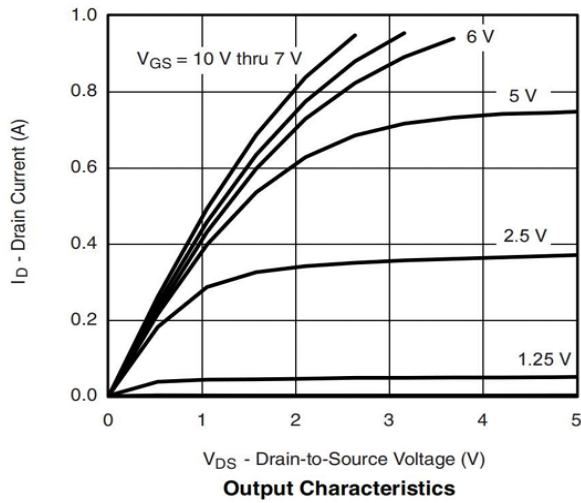
- The value of $R_{\theta\text{JA}}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user is specific board design. The power dissipation is based on the $t\leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_{D} is based on $T_{\text{J(MAX)}}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

➤ **Electrical Characteristics (T_A=25°C unless otherwise noted)**

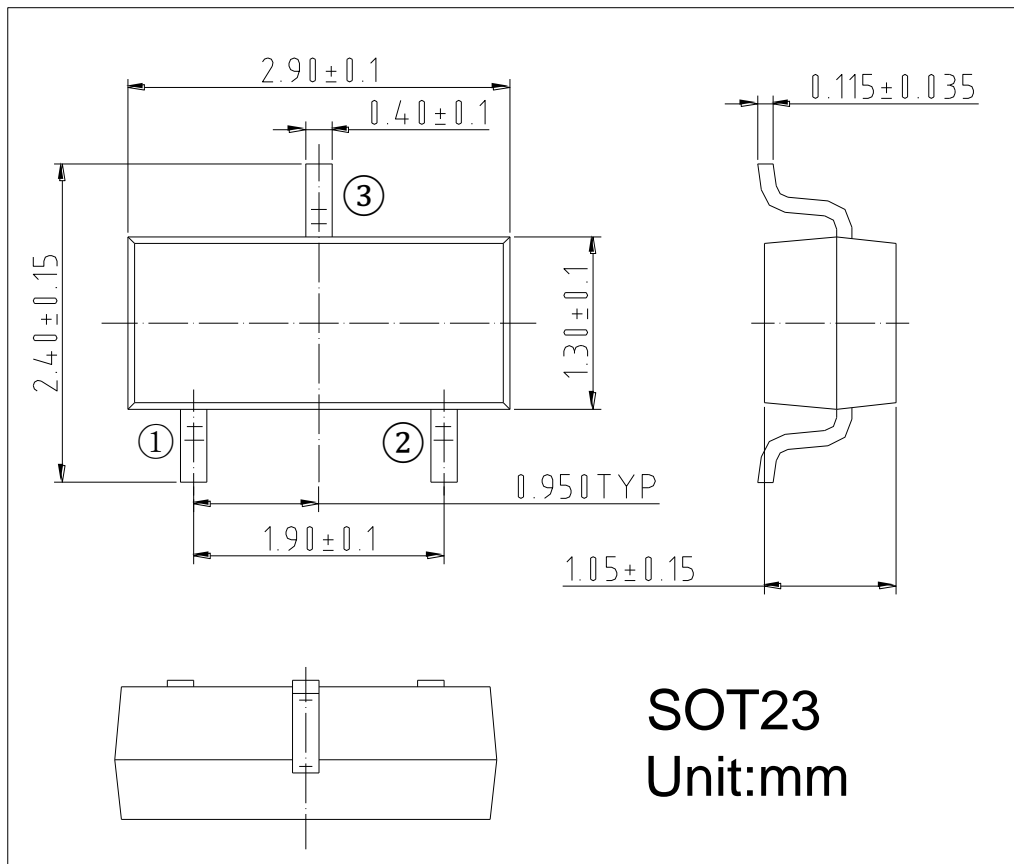
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	0.6	1	1.25	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 0.5A		1.1	2.5	Ω
		V _{GS} = 4.5V, I _D = 0.5A		1.5	3.5	
		V _{GS} = 2.5V, I _D = 0.2A		1.7	4	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	I _{GSS}	V _{GS} = ±12V, V _{DS} = 0V			±10	μA
Transconductance	G _{FS}	V _{DS} = 10V, I _D = 0.2A		0.1		s
Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = 0.2A			1.3	V
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		32		pF
Output Capacitance	C _{OSS}			6.3		
Reverse Transfer Capacitance	C _{RSS}			2.9		
Turn-on Delay Time	T _{D(ON)}	V _{GS} = 10V, V _{DS} = 10V, I _D = 0.1A		26		ns
Rise Time	T _r			10.5		
Turn-off Delay Time	T _{D(OFF)}			37		
Fall Time	T _f			21		
Total Gate Charge	Q _G	V _{GS} = 10V, V _{DS} = 15V, I _D = 0.2A		0.4		nC
Gate to Source Charge	Q _{GS}			0.1		
Gate to Drain Charge	Q _{GD}			0.11		



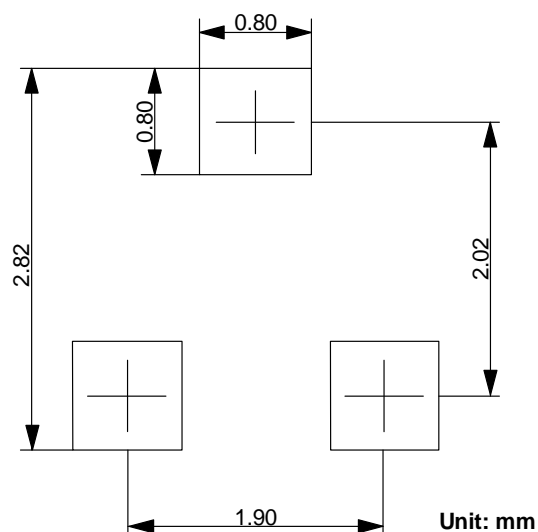
➤ Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



➤ Package Information



➤ Suggested Pad Layout





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